What is claimed is:

1. A system comprising:

a processor;

a memory coupled to the processor;

a request history buffer coupled to the processor;

a pre-fetch control unit coupled to the request history buffer, wherein the pre-fetch control unit to check the request history buffer for a flag associated with a second memory location that is based on a first memory location called by the processor;

a pre-fetcher coupled to the memory to pre-fetch data associated with the second memory location from the memory if no flag associated with the second memory location is in the request history buffer.

2. The system of claim 1, further comprising:

a pre-fetch cache coupled to the pre-fetcher, wherein the pre-fetch cache is to store the pre-fetched data associated with the second memory location.

3. The system of claim 2, wherein the pre-fetcher is to pre-fetch data associated with the second memory location from the memory if data associated with the second memory location is not in the pre-fetch cache.

4. The system of claim 2, wherein the pre-fetcher is to pre-fetch data from a third memory location if data from the second memory location is flagged in the request history buffer or present in the pre-fetch cache, wherein the third memory location is based on the first memory location and the second memory location.

5. The system of claim 4, wherein the pre-fetcher is to pre-fetch data in a stream-up direction.

6. The system of claim 4, wherein the pre-fetcher is to pre-fetch data in a stream-down direction.

7. The system of claim 2, wherein the pre-fetcher is to store a flag, associated with data in the second memory location, in the request history buffer if the data in the second memory location is called.

8. An apparatus for pre-fetching data comprising:

a cache;

a pre-fetch cache coupled to the cache;

a memory, wherein a first data with a first data address is called from the memory and stored in the cache;

a request history buffer (RHB) coupled to the prefetch cache, the RHB to store a flag indicating whether the first data has been called from the memory;

a pre-fetcher to fetch data associated with an initial guess pre-fetch address responsive to the first data to search the cache and to generate a second data address, wherein the pre-fetcher is to fetch a second data associated with the second data address from the memory and to store the second data in the pre-fetch cache; and

a pre-fetch control unit to coordinate the flag stored in the RHB, wherein the pre-fetch control unit is responsive to the pre-fetcher.

9. The apparatus of claim 8, wherein the initial guess prefetch address is numerically higher than that of the first data address.

10. The apparatus of claim 8, wherein the second data address is equal to the initial guess prefetch address when the initial guess prefetch address is not found in the cache.

11. The apparatus of claim 8, wherein the second data address is numerically lower than the initial guess pre-fetch address if the initial guess prefetch address is found in the pre-fetch cache.

12. The apparatus of claim 8, wherein the pre-fetch cache is to be searched for the first data, before the first data is called from the memory.

13. The apparatus of claim 8, wherein the RHB is responsive to a two-sector cache.

14. The apparatus of claim 8, wherein the pre-fetch cache is a content addressable memory (CAM) cache.

15. The apparatus of claim 8, further comprising:

a sector number reader to read a user-set value "N" and wherein the RHB is responsive to an N-sector cache.

16. The apparatus in accordance with claim 8, wherein the pre-fetch cache is larger than the RHB.

17. A system comprising:

a memory;

a processor coupled to the memory, wherein the processor is to call data from a first memory location in the memory;

a request history buffer to store a flag associated with the first memory location, wherein the flag indicating that the data associated has been called by the processor;

a pre-fetch control unit to check for a flag associated with data from a second memory location in the request history buffer, wherein the second memory location is calculated by shifting the first memory location by N in a first direction;

a pre-fetch cache; and

a pre-fetcher to pre-fetch data from the second memory location in the memory and store it in the pre-fetch cache, if data from the second memory location is not flagged in the request history buffer or present in the pre-fetch cache.

18. The system of claim 17, wherein the pre-fetcher is to pre-fetch data from a third memory location, wherein the third memory location is to be calculated by shifting the first memory location by N in a second direction opposite to the first direction, if data from the second memory location is flagged in the request history buffer or present in the pre-fetch cache.

19. (New) The system of claim 17, further comprising:

a cache to store the data called by the processor.